Thin Solid Films 520 (2012) 6681–6683

Contents lists available at SciVerse ScienceDirect

Thin Solid Films

journal homepage: www.elsevier.com/locate/tsf

High performance self-aligned top-gate ZnO thin film transistors using sputtered Al_2O_3 gate dielectric☆

Rongsheng Chen *, Wei Zhou, Meng Zhang, Hoi Sing Kwok

Center for Display Research, Department of Electronic and Computer Engineering, Hong Kong University of Science and Technology, Clear Water Bay, Kowloon, Hong Kong

ARTICLE INFO

Article history:
Received 3 February 2012
Received in revised form 31 May 2012
Accepted 24 June 2012
Available online 29 June 2012

Keywords:
Aluminum oxide
Self-aligned structure
Thin film transistors
Zinc oxide

ABSTRACT

High performance self-aligned top-gate zinc oxide (ZnO) thin film transistors (TFTs) utilizing high-*k* Al_2O_3 thin film as gate dielectric are developed in this paper. Good quality Al_2O_3 thin film was deposited by reactive DC magnetron sputtering technique using aluminum target in a mixed argon and oxygen ambient at room temperature. The resulting transistor exhibits a field effect mobility of 27 cm^2/V s, a threshold voltage of −0.5 V, a subthreshold swing of 0.12 V/decade and an on/off current ratio of 9×10^6. The proposed top-gate ZnO TFTs in this paper can act as driving devices in the next generation flat panel displays.

1. Introduction

Zinc oxide (ZnO) has attracted wide attention with its notable advantages over the other semiconductors including a wide direct band gap of 3.37 eV, high transparency in the visible range (400–700 nm), good thermal stability, large exciton binding energy (60 meV) and high mobility. Therefore, ZnO thin film transistors (TFTs) have become attractive for use as driving devices in large scale active matrix organic light emitting diode applications, due to their better reliability and performance including high mobility, excellent subthreshold gate voltage swing, and high on/off current ratios, as compared to a-Si TFTs [1–4]. The ZnO TFTs have better electrical performance uniformity than the poly-Si TFTs due to the different grain size and grain boundaries in the poly-Si thin films. A bottom-gate structure for ZnO TFT is widely studied. However, this structure is unsuitable for the realization of complementary metal-oxide-semiconductor gates for digital and analog circuits because it has a high parasitic capacitance and poor scalability. Therefore, the development of a self-aligned top-gate ZnO TFT is necessary.

A number of gate dielectrics have been investigated for ZnO-based TFTs, such as HfO_2 [3], SiO_2 [5], Si_3N_4 [6], Y_2O_3 [7], Al_2O_3 [8,9] and so on. Due to its low interfacial trap density with oxide semiconductors and a high relative permittivity of ~9, Al_2O_3 is a promising gate dielectric. The oxide TFT using Al_2O_3 gate dielectric fabricated by atomic layer deposition, exhibits remarkably high and stable performance. However, the exclusive atomic layer deposition system and extremely low deposition rate would increase the manufacturing cost.

For the mass production in industry, Al_2O_3 thin film deposited by magnetron sputtering technique has the potential of high deposition rate, large area, good uniformity and low cost. In this paper, Al_2O_3 thin film deposited by reactive DC magnetron sputtering and its application to ZnO TFTs has been developed. Due to good insulating property and a relative permittivity of 7.2 for this Al_2O_3 gate dielectric, the resulting transistor exhibits a field effect mobility of 27 cm^2/Vs, a threshold voltage of −0.5 V, a subthreshold swing of 0.12 V/decade and an on/off current ratio of 9×10^6.

2. Experimental details

Al_2O_3 thin film was deposited by reactive DC magnetron sputtering technique using aluminum target in a mixed argon and oxygen ambient at room temperature. The deposition pressure and the power were 0.26 Pa and 120 W, respectively. In order to study the electrical characteristics of Al_2O_3 thin film, capacitor formed by $Si/Al_2O_3/Al$ structure with a thickness of 54 nm and an area of 50 μm × 50 μm was measured at a frequency of 1 kHz using an HP 4284A LCR meter. The morphology of roughness of the Al_2O_3 thin film surfaces was observed by atomic force microscope (AFM) (XE-150 S, Park Systems) under non-contact mode using Applied Nano silicon tip with the normal resonant frequency of 300 kHz.

The cross-sectional schematic of the self-aligned top-gate type ZnO TFT studied in this paper is shown in Fig. 1. A 80 nm thick ZnO active layer was first sputtered on thermally oxidized silicon wafer by radio frequency magnetron sputtering (120 W) using a single ZnO target in a mixed argon and oxygen ambient ($Ar:O_2 = 9:1$) at

☆ This research is supported by Hong Kong Government Research Grants Council Grant Number 614410.

* Corresponding author. Tel.: +852 2358 7085; fax: +852 2358 1485.
E-mail address: rschen@ust.hk (R. Chen).

0040-6090/$ – see front matter © 2012 Elsevier B.V. All rights reserved.
doi:10.1016/j.tsf.2012.06.066

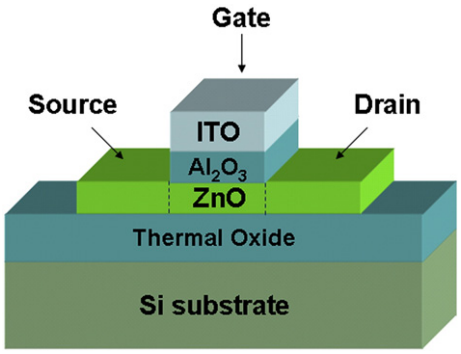

Fig. 1. A cross-section schematic of the proposed ZnO TFT with self-aligned top-gate structure.

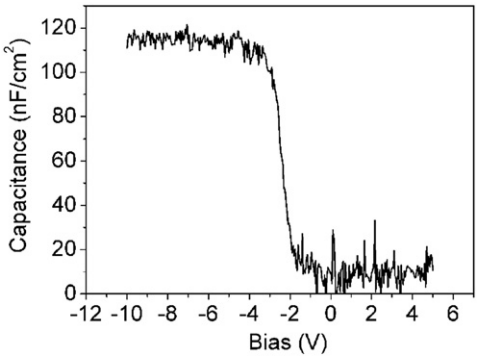

Fig. 3. Capacitance density of the Si/Al_2O_3/Al capacitor.

room temperature. After patterning this ZnO active layer by lift-off process, a 100 nm thick Al_2O_3 layer was deposited by DC sputtering at room temperature on top of the active layer. A 100 nm thick indium tin oxide (ITO), used as gate electrode because of the required work function and optical transparency, was sequentially sputtered at room temperature. The ITO gate electrode and Al_2O_3 gate dielectric were defined by one mask using photolithography and lift-off process. The device was then annealed at 400 °C for 30 minutes in O_2 and N_2 ambient.

Under 3 minute trifluoromethane CHF_3/O_2 plasma treatment, the source/drain regions were formed, self-aligned and doped n-type by hydrogen element, which lead to a low sheet resistance and a low contact resistance between the source/drain electrodes and the channel of the active layer. The electrical properties of the TFTs were measured using an Agilent 4145B parameter analyzer.

3. Results and discussion

The atomic force microscope (AFM) image of Al_2O_3 film is shown in Fig. 2. The root mean square surface roughness is about 0.3 nm, which implicates the smooth surface of Al_2O_3 gate dielectric.

Fig. 3 shows the measured capacitance density of Si/Al_2O_3/Al capacitor, which is about 117 nF/cm^2. The relative permittivity of this Al_2O_3 thin film is estimated to be 7.2. The breakdown electric field of this Al_2O_3 film is about 4 MV/cm, which is higher than that of rf sputtered Al_2O_3 [10]. This high breakdown electric field implicates that this DC sputtered Al_2O_3 film has less pin holes than that deposited by rf sputtering process. However, it is still lower than that of SiO_2 (10 MV/cm). For the reliability issue, there is small shift over long term operation due to charge trapping in the dielectric.

The field effect mobility induced by the transconductance at a low drain voltage is given by

$$\mu_{FE} = \frac{Lg_m}{WC_{OX}V_{DS}} \quad (1)$$

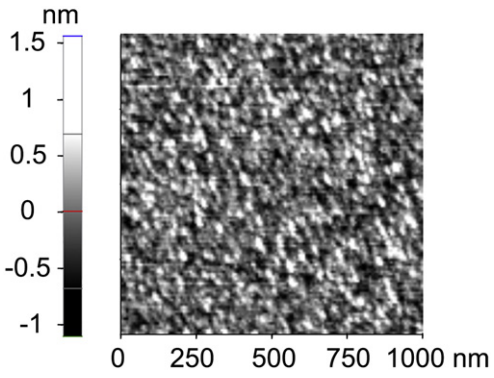

Fig. 2. An AFM image for Al_2O_3 thin film deposited by sputtering.

where g_m and C_{OX} are the transconductance and the gate insulator capacitance per unit area, respectively. Fig. 4 shows the typical transfer and output characteristics of the fabricated ZnO TFTs. They exhibit good transfer TFT characteristics at V_{DS} of 0.1 V such as a field effect mobility of 27 cm^2/Vs, a threshold voltage of −0.5 V, a subthreshold swing of 0.12 V/decade and an on/off current ratio of 9×10^6. The saturate mobility of about 30 cm^2/Vs is also obtained at a $V_{DS}=5$ V. The linear mobility and saturate mobility obtained are nearly comparable, implying that the field effect mobility is independent on drain voltage. The output characteristic shows clear linear regions and does not show significant current crowding at low V_{DS}, indicating that low series resistance in source/drain contacts was obtained. The source/drain series resistance (R_{SD}) was also extracted by determining the device on-resistance R_{on} from the linear region of the transfer characteristics and plotting the width normalized $R_{on}W$ as a function of the channel length (L) for different gate voltages [11]. Fig. 5 shows the width normalized $R_{on}W$ as a function of L at different gate voltage at $V_{DS}=0.1$ V for the ZnO TFTs. The $R_{SD}W$ for the ZnO TFTs, which is extracted at the y-axis intercept of the extrapolated linear fit of $R_{on}W$ versus L, is approximately 75 Ω-cm for different gate voltage.

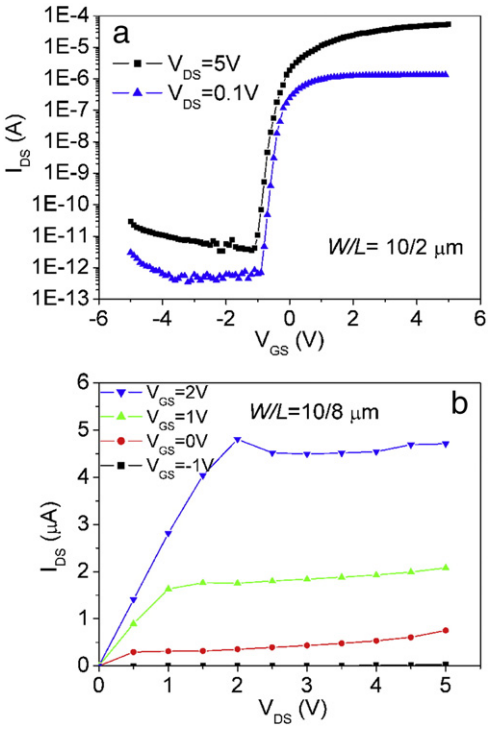

Fig. 4. (a) Transfer characteristic and (b) output characteristic of the proposed self-aligned top-gate ZnO TFT.

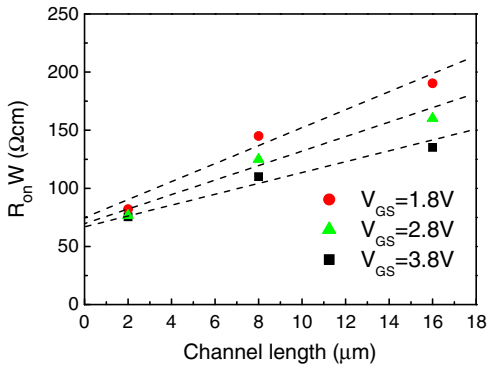

Fig. 5. Width-normalized device on resistance $R_{on}W$ as a function of L.

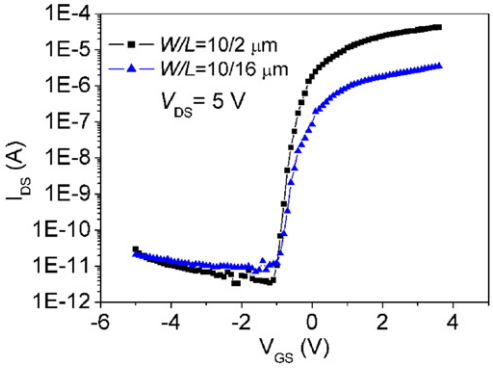

Fig. 6. Transfer characteristics of the ZnO TFTs with the same channel width $W = 10$ μm but different lengths $L = 16$, 2 μm.

The transfer characteristic (at $V_{DS} = 5$ V) of the ZnO TFTs with different channel lengths ($L = 16$, 2 μm) is compared in Fig. 6. From Fig. 6, small change of the threshold voltages and little shift of subthreshold swing with different channel lengths were obtained, which indicates good stability against short channel effects. This characteristic is much better than that reported earlier for devices with an inverted staggered, bottom-gate structure [12].

4. Conclusion

Due to good insulating property and a relative permittivity of 7.2 for this Al_2O_3 gate dielectric, high performance self-aligned top-gate ZnO thin film transistors are developed in this paper. With scaling down the channel length, good characteristics are also obtained with small change of the threshold voltages and no degradation of subthreshold swing. The proposed top-gate ZnO TFTs in this paper can act as driving devices in the next generation flat panel displays.

References

[1] R.L. Hoffman, B.J. Norris, J.F. Wager, Appl. Phys. Lett. 82 (2003) 733.
[2] E.M.C. Fortunato, P.M.C. Barquinha, A.C.M.B.G. Pimentel, A.M.F. Goncalves, A.J.S. Marques, R.F.P. Martins, L.M.N. Pereira, Appl. Phys. Lett. 85 (2004) 2541.
[3] J.H. Kim, B. Du Ahn, C.H. Lee, K.A. Jeon, H.S. Kang, S.Y. Lee, Thin Solid Films 516 (2008) 1529.
[4] W.S. Choi, J. Soc. Info. Display 17 (2009) 751.
[5] M.G. McDowell, I.G. Hill, IEEE Trans. Electron Devices 56 (2009) 343.
[6] I. Song, S. Kim, H.X. Yin, C.J. Kim, J. Park, S. Kim, H.S. Choi, E. Lee, Y. Park, IEEE Electron Device Lett. 29 (2008) 549.
[7] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, H. Hosono, Nature 432 (2004) 488 (London).
[8] J.B. Kim, C. Fuentes-Hernandez, W.J. Potscavage, X.H. Zhang, B. Kippelen, Appl. Phys. Lett. 94 (2009) 142107.
[9] L.F. Lan, J.B. Peng, IEEE Trans. Electron Devices 58 (2011) 1452.
[10] M. Voigt, A. Bergmaier, G. Dollinger, M. Sokolowski, J. Vac. Sci. Technol., A 27 (2009) 234.
[11] J. Zaumseil, K.W. Baldwin, J.A. Rogers, J. Appl. Phys. 93 (2003) 6117.
[12] H.H. Hsieh, C.C. Wu, Appl. Phys. Lett. 89 (2006) 041109.